WE CLAIM:

1. An apparatus for suppressing noise in an electrical device, the apparatus comprising:

a first conductive layer;

a second conductive layer separated from the first conductive layer;

first conductive rods connected to the second conductive layer and extending to the first conductive layer; and

chip capacitors connected to the first conductive rods and arranged in a lattice.

2. The apparatus of claim 1 wherein the chip capacitors connect the first conductive rods to the first conductive layer.

3. The apparatus of claim 1 wherein the chip capacitors are arrayed over substantially an entire area of the first conductive layer.

4. The apparatus of claim 1 further comprising a first dielectric layer disposed between the first and second conductive layers and through which the first conductive rods pass.

5. The apparatus of claim 4 further comprising a third conductive layer disposed on an opposite side of the second conductive layer as the first conductive layer and a second dielectric layer disposed between the second and third conductive layers.

6. The apparatus of claim 5 wherein the first conductive rods pass through the second dielectric layer and extend to the third conductive layer, the chip capacitors are arranged in a lattice on the first and third conductive layers and connect the first conductive rods to the first and third conductive layers, respectively.

7. The apparatus of claim 1 wherein the first conductive rods comprise plated vias.

8. The apparatus of claim 7 wherein the first conductive layer houses pads to which the conductive rods and chip capacitors are connected, and a clearance space is disposed between the pads and metal of the first conductive layer.

9. The apparatus of claim 1 further comprising a lattice of conductive coplanar patches disposed between the first and second conductive layers.

10. The apparatus of claim 9 wherein the patches are connected with the second conductive layer and the chip capacitors through the first conductive rods.

11. The apparatus of claim 10 wherein each patch is connected to one of the chip capacitors through one of the first conductive rods.

12. The apparatus of claim 10 further comprising a third dielectric layer disposed between the patches and the second conductive layer and a fourth dielectric layer disposed between the patches and the first conductive layer.

13. The apparatus of claim 10 wherein at least one lattice of the chip capacitors and the patches are arrayed over substantially an entire area of the first conductive layer.

14. The apparatus of claim 13 wherein both the lattice of the chip capacitors and the patches extend over substantially the entire area of the first conductive layer.

15. The apparatus of claim 1 further comprising:

a fourth conductive layer disposed between the first and second conductive layers and which is at a different potential from the second conductive layer; and

second conductive rods connected to the fourth conductive layer and extending to the first conductive layer,

wherein the chip capacitors connect the first conductive rods to the second conductive rods.

16. The apparatus of claim 15 wherein the chip capacitors are arrayed over substantially an entire area of the first conductive layer.

17. The apparatus of claim 15 further comprising a fifth dielectric layer disposed between the second and fourth conductive layers and through which the first conductive rods pass and a sixth dielectric layer disposed between the first and fourth conductive layers and through which the first and second conductive rods pass.

18. The apparatus of claim 17 further comprising a fifth conductive layer disposed on an opposite side of the second conductive layer as the first conductive layer and a seventh dielectric layer disposed between the second and fifth conductive layers.

19. The apparatus of claim 18 wherein the first conductive rods pass through the seventh dielectric layer and extend to the fifth conductive layer, the second conductive rods pass through the fifth and seventh dielectric layers and extend to the fifth conductive layer.

20. The apparatus of claim 19 wherein the chip capacitors are arranged in a lattice only one of the first and fifth conductive layers.

21. The apparatus of claim 19 wherein the chip capacitors are arranged in a lattice on both the first and fifth conductive layers.

22. The apparatus of claim 15 further comprising a lattice of conductive coplanar patches disposed between the first and second conductive layers.

23. The apparatus of claim 22 wherein the patches are closer to the fourth conductive layer than the second conductive layer.

24. The apparatus of claim 22 wherein the patches are connected with the second conductive layer and the chip capacitors through the first conductive rods.

25. The apparatus of claim 24 further comprising an eight dielectric layer disposed between the patches and the second conductive layer and through which the first conductive rods pass, a ninth dielectric layer disposed between the first and fourth conductive layers and through which the first and second conductive rods pass, and a tenth dielectric layer disposed between the patches and the fourth conductive layer.

26. The apparatus of claim 25 wherein at least one lattice of the chip capacitors and the patches are arrayed over substantially an entire area of the first conductive layer.

27. The apparatus of claim 26 wherein both the lattice of the chip capacitors and the patches extend over substantially the entire area of the first conductive layer.

28. The apparatus of claim 25 further comprising a sixth conductive layer disposed on an opposite side of the second conductive layer as the first conductive layer and an eleventh dielectric layer disposed between the second and sixth conductive layers.

29. The apparatus of claim 28 wherein the first conductive rods pass through the eleventh dielectric layer and extend to the sixth conductive layer, the

second conductive rods pass through the eight and eleventh dielectric layers and extend to the sixth conductive layer.

30. The apparatus of claim 29 wherein the chip capacitors are arranged in a lattice only one of the first and sixth conductive layers.

31. The apparatus of claim 30 wherein the chip capacitors are arranged in a lattice on both the first and sixth conductive layers.

32. A printed circuit board (PCB) comprising:

a power distribution network including a periodic structure integral with a parallel-plate waveguide operative to define a fundamental stopband over a range of frequencies, the periodic structure including:

a first conductive layer,

a second conductive layer,

an array of conductive coplanar patches more proximate to the first conductive layer than the second conductive layer,

dielectric layers separating the layers,

conductive rods connected to the second conductive layer and extending through the first conductive layer, and

an array of chip capacitors disposed over substantially the entirety of the first conductive layer, the chip capacitors connecting the conductive rods with metal of the first conductive layer,

wherein at least a capacitance formed by the patches and the first conductive layer, a capacitance of the array of chip capacitors, and inductance of the rods are selected to optimize suppression of noise over the at least one stopband.

33. The PCB of claim 32 wherein a lower edge of the fundamental stopband is less than 100 MHz for a unit cell area of the array of less than about 0.1 square inches.

34. The PCB of claim 32 wherein an average of a maximum attenuation of the PCB in the fundamental stopband from about 100 MHz to 2 GHz is at least about 40 dB for locations separated by at least 7 unit cells compared with a PCB that does not contain the array of patches and the array of chip capacitors.

35. A printed circuit board (PCB) comprising:

a first signal layer disposed on an outer surface of the PCB;

a ground plane;

a power plane;

an array of conductive coplanar patches more proximate to the power plane than the ground plane;

dielectric layers separating the ground and power planes, the signal layer; and the patches;

an array of capacitors disposed on the first signal layer;

first pads disposed on the first signal layer and on which the capacitors are mounted; and

first plated through holes connecting the ground plane and patches with the pads and capacitors.

36. The PCB of claim 35 further comprising second pads disposed on the first signal layer and on which the capacitors are mounted and second plated through holes connecting the power plane with the second pads and capacitors, wherein the first and second pads are separated from each other.

37. The PCB of claim 35 further comprising:

a second signal layer disposed on another outer surface of the PCB;

third pads disposed on the second signal layer; and

third plated through holes connecting the third pads with the ground plane.

38. The PCB of claim 37 further comprising an array of capacitors disposed on the second signal layer and mounted on the third pads.

39. The PCB of claim 35 wherein the capacitors are connected to signal lines on the first signal layer.

40. The PCB of claim 36 further comprising:

a second signal layer disposed on another outer surface of the PCB;

fourth pads disposed on the second signal layer; and

fourth plated through holes connecting the fourth pads with the ground plane.

41. The PCB of claim 40 further comprising an array of capacitors disposed on the second signal layer and mounted on the fourth pads.

42. The PCB of claim 41 further comprising fifth pads disposed on the second signal layer and on which the capacitors are mounted and fifth plated through holes connecting the power plane with the fifth pads and capacitors, wherein the fourth and fifth pads are separated from each other.

43. A method for suppressing noise in a printed circuit board (PCB), the method comprising selecting locations of the PCB between which suppression of the noise is desired, arranging a plurality of unit cells of a lattice of chip capacitors between the locations, and mounting the capacitors on the PCB such that one end of the capacitors are grounded.

44. The method of claim 43 further comprising mounting an opposing end of the capacitors such that the capacitors are connected with a power plane.

45. The method of claim 43 further comprising mounting an opposing end of the capacitors such that the capacitors are connected with signal lines of the PCB.

46. The method of claim 43 further comprising arranging a lattice of buried patches between the locations under the lattice of capacitors.

47. The method of claim 46 further comprising providing substantially the same number of patches and capacitors and arranging the patches such that the patches and capacitors are substantially in one-to-one correspondence with each other.